REMARKS

Claim 6 is amended to make it depend on claim 5 rather than claim 1 because the antecedent basis for "second means" recited in claim 6 is in claim 5, not claim 1.

The following numbered sections of the applicant's remarks are provided in response to similarly numbered sections of the office action.

1. Claim 4 is amended in response to the Examiner's objection.

2. Claim 12 is amended in response to the Examiner's objection.

3. Claims 12 is amended in response to the Examiner's objection.

4. No comment is necessary.

5. Claim 1 is rejected under 35 U.S.C. 102 as being anticipated by U.S. Patent 5,948,115 (Dinteman). The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

Dinteman teaches that when a circuit is supposed to tolerate a specified amount of jitter in an input signal, an IC tester can test the IC's jitter tolerance by adding a controlled amount of jitter to the IC input signal and then monitoring the IC's output signals to see whether they behave as expected. Dinteman's jitter generator (FIG. 6) includes a programmable delay circuit 54 controlled by data (DELAY) produced by a pattern generator 56. The delay circuit delays a timing signal TD to produce a delayed timing signal TD' applied to a shift-out terminal of a FIFO buffer 52 producing a signal (DRIVE) driving a tristate buffer 42 (FIG. 6) producing an output TEST signal supplied as input to an IC. Varying the value of DELAY during each test cycle causes the timing of state changes in the TEST signal to vary from cycle-to-cycle. Note that the rate at which pattern generator 56 changes the DELAY data input to the delay circuit 54 matches the frequency of the TEST signal. Thus Dinteman's programmable delay

circuit delays one timing signal TD to produce another timing signal TD' and does not directly produce a test signal supplied to an IC under test.

The applicant's claim 1 (as amended) recites a jitter generator including a programmable delay circuit for delaying a first signal to produce a test signal directly supplied to the IC and "first means" for supplying a digital sequence for controlling the delay circuit's delay so that test signal jitters.

Claim 1 is patentable over Dinteman because the output signal TD' of Dinteman's programmable delay circuit is not the "jittery test signal for use in the IC" as recited in claim 1, but is instead a timing signal for use only within the IC tester.

6. No comment is necessary.

7. No comment is necessary.

8. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman and U.S. Patent 6,006,347 (Churchill). The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman as teaching the underlying subject matter of claim 1 and cites Churchill as teaching the additional limitations of claims 2 and 3. Claims 2 and 3 are patentable over the combination of Dinteman and Churchill because, as discussed above relative to claim 1, Dinteman fails to teach limitations of claim 1.

One drawback to Dinteman's approach to adding jitter to a test signal is that noise in the signal path conveying the test signal from the tester to the IC can introduce additional jitter into the test signal so that the actual jitter in the test signal arriving at the IC can vary from the controlled amount added by the tester. The applicant's claim 2 recites that the programmable delay circuit resides within the IC itself, and is therefore not subject to noise in the signal path from the tester. Dinteman's programmable delay

circuit resides within an IC tester, but the Examiner points to Churchill (Fig. 3) as showing a programmable delay circuit 302 embedded in an IC for delaying a circuit input signal 314 by an amount controlled by data supplied by a scan register 306 to produce a signal 316.

In order to produce jitter in a test signal (such as signal 316) it is necessary to supply control data to programmable delay circuit 302 that changes at the rate at which state changes in the test signal occur because it is necessary to independently control the timing of each edge of the test signal. The data in Churchill's scan register 306 which controls delay circuit 302 is serially shifted into the scan register 306 via a scan bus. A scan bus is typically used during testing to shift data in and out of registers within an IC under test, but not when the IC is processing input signals at their rated frequency, as would be the case during a jitter test. To use a scan bus, an IC test is halted, data is shifted in and out of the IC via the scan bus to change control settings or to view states of internal IC signals, and the test is then resumed. One of skill in the art would therefore not be motivated to use Churchill's programmable delay circuit 302 to produce a jittery test signal for use in jitter testing because the scan bus could not supply data to frequency modulate input signal 314 at a sufficient rate during a test when the IC is processing the jittery test signal 316.

Claim 3 is patentable over the combination of Dinteman and Churchill for similar reasons.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Churchill and U.S. Patent 5,796,745 (Adams). The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman and Churchill as teaching the underlying subject matter of claim 3 and cites Adams only as teaching that a programmable pattern generator can be embedded in an IC, the additional limitations of claim 4. Claim 4 is patentable over the

combination of Dinteman and Churchill and Adams because, as discussed above relative to claim 3, Dinteman and Churchill fail to teach limitations of claim 3.

Adams teaches a BIST circuit within an IC including a programmable pattern generator for supplying data input to a memory during a test. The Examiner suggests that Adams would motivate one of skill in the art to embed the pattern generator 56 of Dinteman in the TC being tested rather than place it in the IC tester. However note that Dinteman's pattern generator 56 (FIG. 6) supplies control data (DELAY) to a delay circuit 54 inside the tester that produces a timing signal TD', also used inside the tester. Pattern generator 56 does not supply control data to a delay circuit that is inside the IC and which produces a test signal used inside the IC. Thus one of skill in the art would not be motivated to embed Dinteman's pattern generator 56 in the IC under test since it would render Dinteman's test circuit non-functional. The DELAY data and the TD' signal it controls are needed inside the tester, not inside the IC being tested.

Claim 4 is therefore patentable over the cited references.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Churchill, Adams and U.S. Patent 5,815,512 (Osawa). The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman, Churchill and Adams as teaching the underlying subject matter of claim 4 and cites Osawa only as teaching to selectively apply either the first signal or the test signal as an input signal to the subcircuit. Claim 5 is patentable over the combination of Dinteman, Churchill, Adams and Osawa because, as discussed above relative to claim 4, Dinteman, Churchill and Adams fail to teach limitations of claim 4.

The Examiner cites Osawa (FIG. 1) as showing a selector circuit 233 (which is also called a multiplexer) that can selectively supply either of its two input signals as an output signal. Osawa's selector 233 is included in a scan register to select between a data signal

output D of a semiconductor device and a serial signal SI from an external source. Osawa's circuit has nothing to do with jitter testing and does not select between the input to a programmable delay circuit and the jittery output of the programmable delay circuit as recited in the applicant's claim 5. Thus Osawa provides no motivation for one of skill in the art to use Osawa's selector in connection with Dinteman's jitter generator circuit. Claim 5 is therefore patentable over the cited references.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman and Osawa. The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

Claim 6 is amended to make it depend on claim 5 rather than claim 1 since "the second means" to which claim 6 refers is introduced in claim 5, not claim 1. Applicant assumes that with such an amendment the Examiner would have rejected claim 6 under the combination of Dinteman, Churchill, Adams and Osawa as applied against clam 5. Claim 6 (as amended) is patentable over that combination of references for reasons discussed above in connection with its parent claim 5.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Churchill, Adams, Osawa, and U.S. Patent 6,501,693 (Takatsuka). The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman, Churchill, Adams and Osawa as teaching the underlying subject matter of claim 5 and cites Takatsuka only as teaching the "second means" recited in claim 7. Claim 7 is patentable over the combination of Dinteman, Churchill, Adams, Osawa and Takatsuka because, as discussed above relative to claim 5, Dinteman, Churchill, Adams and Osawa fail to teach limitations of claim 5.

The Examiner cites the following lines from a claim of Takatsuka that appear to relate to selector circuit 62 of Takatsuka's FIG. 3 which, according to Takatsuka (col. 9, lines 1-11), is "for outputting

either signal INTSIG or ZRXTRST as a signal ZRXTRSTD in accordance with test signal TEST". Thus it appears that a test signal is controlling Takatsuka's selector 62 and is not one of the input signals that the selector is selecting, as is the case for the applicant's "second means" recited in claim 7. Claim 7 is therefore patentable over the cited references.

13. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Churchill, Adams, Osawa, Takatsuka and U.S. Patent 6,463,693 (Bhawmik). The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman, Churchill, Adams, Osawa and Takatsuka as teaching the underlying subject matter of claim 7 and cites Bhawmik only as teaching the "third means" recited in claims 8 and 9. Claims 8 and 9 are patentable over the combination of Dinteman, Churchill, Adams, Osawa, Takatsuka and Bhawmik because, as discussed above relative to claim 7, Dinteman, Churchill, Adams, Takatsuka and Osawa fail to teach limitations of claim 7.

Claims 8 and 9 further recite "third means residing within the IC for generating the first signal". Thus the "first signal" that is variably delayed to produce the jittery test signal is generated within the IC too. The Examiner cites Bhawmik (col. 1, lines 16-23) as teaching generating test signals inside an IC, but nothing in Bhawmik indicates that such an internally generated test signal should be applied as input to a programmable delay circuit within the IC which adds a controlled amount of jitter to the test signal. Also since Dinteman teaches to variably delay a timing signal used in an IC tester, rather than a test signal, Bhawmik would not motivate one of skill in the art to move Dinteman's pattern generator from the tester to the IC being tested. Claims 8 and 9 are therefore patentable over the cited references.

14. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman and U.S. Patent 6,535,014 (Chetlur). The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman as teaching the underlying subject matter of claim 1 and cites Chetlur as teaching additional limitations of claims 10 and 11. Claims 10 and 11 are therefore patentable over the combination of Dinteman and Chetlur because, as discussed above relative to claim 1, Dinteman fails to teach limitations of claim 1.

Claims 10 and 11 further recite a multiplexer that can feed the test signal output of the programmable delay circuit back to the input of the programmable delay circuit so that the test signal oscillates. See the applicant's FIG. 4. This allows the circuit to generate an oscillating test signal for calibration purposes without deriving it from the IC input signal VIN. The VIN signal, which comes from an IC tester, would have noise that would adversely affect delay circuit calibration.

The Examiner correctly points out that Dinteman does not disclose such a multiplexer that allows the output signal T' of delay circuit 54 to be fed back to its input.

The Examiner points to Dinteman (col. 5, lines 45-46, col. 6, lines 16-20, col. 6, lines 30-34) as teaching a test signal that oscillates with a period that is a function of the delay provided by the programmable delay circuit when the test signal output of the programmable delay circuit is fed back to the delay circuit's inputs. However col. 5, lines 45-46 teach only that the delay of a programmable delay circuit is specified by its input data, col. 6, lines 16-20 teach that when the delay of the programmable delay circuit is fixed, the DRIVE signal output of buffer 52 (FIG. 6) looks like its D signal input, and col. 6, lines 30-34 simply described the architecture of Dinteman's FIG. 4. Nothing in any of the cited sections of Dinteman mention anything about any signal output of a delay circuit that can be fed back to the delay circuit's input so

that the signal oscillates with a period that is a function of the delay of the delay circuit as recited in claims 10 and 11.

The Examiner cites Chetlur (FIG. 1) as teaching a selector 12 that receives a test signal from a multiplexer 14 and a second signal VG to produce an input signal VIN to a "circuit path", but the selector 12 does not feed back the test signal output of a programmable delay circuit to the delay circuit's input to cause the test signal to oscillate.

Claim 11 recites "third means for generating data that is a function of a period of the test signal when the multiplexer supplies the test signal as the first signal input to the programmable delay circuit". As discussed above, neither Dinteman nor Chetlur teach a multiplexer that feeds a test signal output of a programmable delay circuit back to the delay circuit's input. The Examiner cites Dinteman FIGs. 2 and 6 as teaching a device for generating data that is a function of the TEST signal. However, FIG. 6 shows no device for generating data that is a function of a period of any oscillating test signal supplied to an IC. FIG. 2 shows a compare circuit 28 that generates data that is a function of the output (DUT_OUT) of an IC device under test (DUT). Since the DUT_OUT signal can arrive at the tester on the same bi-directional line that may be used to send a TEST signal to the DUT, the TEST signal appears to be an input to compare circuit 28, but the compare circuit would not generate output FAIL data that is "a function of the period of the test signal as recited in claim 11" even if the compare circuit were used to monitor the TEST signal instead of the DUT_OUT signal. The Examiner cites Dinteman (col. 2, lines 3-38 and col. 6, lines 39-43) as teaching this, but these sections of Dinteman teach nothing about any device that generates data that is a function of the period of a test signal output of an oscillator produced by feeding back the test signal to the input of the oscillator. Claims 10 and 11 are therefore patentable over the cited references.

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Chetlur and Osawa. The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman as teaching the underlying subject matter of claim 1 and cites Chetlur and Osawa as teaching additional limitations of claim 12. Claim 12 is therefore patentable over the combination of Dinteman, Chetlur and Osawa because, as discussed above relative to claim 1, Dinteman fails to teach limitations of claim 1.

The Examiner incorrectly cites Chetlur as teaching the multiplexer of claim 12 as discussed above in connection with claims 10 and 11. Claim 12 is therefore patentable over the cited references.

16. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Chetlur, Churchill, Adams, Osawa, and Takatsuka. The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman, Chetlur and Osawa as teaching the underlying subject matter of claim 12 and cites Churchill and Adams and Osawa as teaching additional limitations of claim 12. Claim 13 is therefore patentable over the combination of Dinteman, Chetlur, Churchill, Adams, Osawa, and Takatsuka. because, as discussed above relative to claim 12, Dinteman, Chetlur, Osawa, and Takatsuka fail to teach limitations of claim 12.

Claim 13 further recites "the programmable delay circuit, the programmable pattern generator, the second means, and the multiplexer reside within the IC."

The Examiner points to Churchill (Fig. 3) as showing a programmable delay circuit 302 residing in an IC for delaying a circuit input signal 314 by an amount controlled by data supplied by a scan register 306 to produce a signal 316. However as discussed above in connection with claim 3, one of skill in the art would not be motivated to use Churchill's programmable delay circuit 302 to produce a jittery test signal because it is controlled by data supplied by a

scan bus that could not supply data to frequency modulate input signal 314 at a sufficient rate when the IC is processing the jittery test signal 316. Thus Churchill would not motivate one of skill in the art to embed Dinteman's programmable delay circuit in the IC being tested.

The Examiner points to Adams as teaching a pattern generator that is embedded in an IC and suggests that Adams would motivate one of skill in the art to embed the pattern generator 56 of Dinteman in the IC being tested rather than place it in the IC tester. However note that Dinteman's pattern generator 56 (FIG. 6) supplies control data (DELAY) to a delay circuit 54 inside the tester that produces a timing signal TD' also used inside the tester. The DELAY data and the TD' signal the pattern generator controls are needed inside the tester because the TD' signal is a timing signal needed to control a part in the tester and is not a test signal supplied to the IC under test. Thus one of skill in the art would not be motivated to embed pattern generator 56 in the IC under test since it would render Dinteman's tester non-functional. Claim 13 is therefore patentable over the cited references.

17. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Chetlur, Churchill, Adams, Osawa, Takatsuka and Bhawmik.

The Examiner cites Dinteman, Chetlur, Osawa and Takatsuka as teaching the underlying subject matter of claim 13 and cites Bhawmik as teaching additional limitations of claim 14. Claim 14 is therefore patentable over the combination of Dinteman, Chetlur, Churchill, Adams, Osawa, Takatsuka and Bhawmik because, as discussed above relative to claim 13, Dinteman, Dinteman, Chetlur, Churchill, Adams, Osawa, and Takatsuka fail to teach limitations of claim 13.

The Examiner cites Bhawmik as teaching the additional limitations of claim 14, the recited "third means residing within the IC for generating data that is a function of a period of the test signal when test signal oscillates". The Examiner cites Bhawmik (col. 1, lines 21-23) as teaching generating test signals inside an IC, but nothing

in Bhawmik indicates that such an internally generated test signal should be applied as input to a programmable delay circuit within the IC which adds a controlled amount of jitter to the test signal. Also since Dinteman teaches to variably delay a timing signal used in an IC tester, rather than a test signal sent to an IC under test, Bhawmik would not motivate one of skill in the art to move Dinteman's pattern generator from the tester to the IC being tested. Claim 14 is therefore patentable over the cited references.

18. Claims 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman and U.S. Patent 5,144,524 (Saxe).

The Examiner cites Dinteman as teaching the underlying subject matter of claim 1 and cites Saxe as teaching the additional limitations of claims 15-21. Claims 15-21 are patentable over the combination of Dinteman and Saxe because, as discussed above relative to claim 1, Dinteman fails to teach limitations of claim 1. The Examiner cites Saxe only as teaching the additional limitations of claims 15-21. Claims 15-21 are therefore patentable over the cited references.

19. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman and Bhawmik. The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

Claim 22 recites that a test signal supplied as input to a subcircuit of an IC being tested is produced at the output of a programmable delay circuit which variably delays a first signal so that the test signal jitters. The Examiner cites Dinteman as teaching this, however the output signal TD' of Dinteman's programmable delay circuit is not a jittery test signal supplied as input to a subcircuit of an IC under test as recited in claim 22 but is instead a timing signal for use within an IC tester for controlling the shift out terminal of FIFO buffer 52. Dinteman's TEST signal, which is supplied to an IC under test, is not the output of Dinteman's programmable delay circuit 54. The Examiner cites Bhawmik only as teaching to

apply a test signal to a subcircuit of an IC under test. Bhawmik would therefore not motivate one of skill in the art to supply the timing signal output TD' of the Dinteman's programmable delay circuit 54 as input to a subcircuit of an IC under test. Claim 22 is therefore patentable over the cited references.

20. Claims 23, 24 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Bhawmik, and U.S. Patent 6,611,477 (Speyer). The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman and Bhawmik as teaching the underlying subject matter of claim 22 and cites Speyer as teaching the additional limitations of claims 23, 24 and 30. Claims 23, 24 and 30 are patentable over the combination of Dinteman Bhawmik and Speyer because, as discussed above relative to claim 22, Dinteman and Bhawmik fail to teach limitations of claim 22.

Claims 23, 24 and 30 further recite that the test signal is fed back to the input of the programmable delay circuit so that the test signal oscillates and then the period of the test signal is measured. The Examiner cites Speyer as teaching an oscillator formed by feeding the output of a delay circuit back to its input, and suggests that one of skill in the art would be motivated to modify Dinteman's circuit in this manner because doing so would provide an oscillating test signal. However since the output of Dinteman's programmable delay circuit is a timing signal TD' and not a test signal, one of skill in the art would not be motivated to modify Dinteman's test circuit in such manner. Doing so would also decouple the timing of the TD' signal from the timing of other circuits within the IC tester which are synchronized to the TD signal, thereby causing the tester channel to loose synchronicity with the other tester channels. One of skill in the art would not want that to happen since all tester channels must be closely synchronized in order to properly test an IC.

Claim 24 further recites "ascertaining values of digital control data included in the sequence supplied at step c needed to produce a

particular jitter pattern in the test signal". The Examiner cites Dinteman (col. 3, lines 25-27 and col. 6, lines 39-48) as teaching this, however while these sections of Dinteman teach only that the control data output of a pattern generator controls the delay of the programmable delay circuit, they do not teach that the proper data values for the pattern generator are determined experimentally from the repetitive measurements of the period of oscillation of the TD' signal when the TD' signal is fed back to the delay circuit input so that it oscillates. Claims 23, 24 and 30 are therefore patentable over the cited references.

21. Claims 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Churchill, and Bhawmik. The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman and Bhawmik as teaching the underlying subject matter of claim 22 and cites Churchill as teaching the additional limitations of claims 25 and 29. Claims 25 and 29 are patentable over the combination of Dinteman, Bhawmik and Churchill because, as discussed above relative to claim 22, Dinteman and Bhawmik fail to teach limitations of claim 22.

The Examiner points to Churchill (Fig. 3) as teaching placing the programmable delay circuit 302 in the IC being tested as recited in claims 25 and 29. However as discussed above in connection with claim 3, one of skill in the art would not be motivated to use Churchill's programmable delay circuit 302 to produce a jittery test signal because it is controlled by data supplied by a scan bus that could not supply data to frequency modulate input signal 314 at a sufficient rate when the IC is processing the test signal 316. Also since Dinteman's programmable delay circuit produces a timing signal used to control a circuit within the tester rather than a test signal supplied to the IC under test, one of skill in the art would not be motivated to embed the programmable pattern generator that supplied state to the delay circuit in the IC. Thus Churchill would not motivate one of

skill in the art to embed Dinteman's programmable delay circuit in the IC being tested. Claims 25 and 29 are therefore patentable over the cited references.

22. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Churchill, Adams, and Bhawmik. The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman, Churchill and Bhawmik as teaching the underlying subject matter of claim 25 and cites Adams as teaching the additional limitations of claim 26. Claim 26 is patentable over the combination of Dinteman, Churchill, Adams, and Bhawmik because, as discussed above relative to claim 25, Dinteman, Churchill and Bhawmik fail to teach limitations of claim 25.

The Examiner points to Adams as teaching a pattern generator embedded in an IC as recited by claim 26 and suggests that Adams would motivate one of skill in the art to embed the pattern generator 56 of Dinteman in the IC being tested rather than place it in the IC tester. However note that Dinteman's pattern generator 56 (FIG. 6) supplies control data (DELAY) to a delay circuit 54 inside the tester that produces a timing signal TD' also used inside the tester. Pattern generator 56 does not supply control data to a delay circuit that is inside the IC and which produces a test signal used inside the IC. The DELAY data and the TD' signal it controls are needed inside the tester because the TD' signal is a timing signal needed to control a part in the tester and is not a test signal supplied to the CI under test. Thus one of skill in the art would not be motivated to embed pattern generator 56 in the IC under test since it would render Dinteman's test circuit non-functional. Claim 26 is therefore patentable over the cited references.

23. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Bhawmik, Churchill, and Saxe. The Examiner

is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman, Churchill and Bhawmik as teaching the underlying subject matter of claim 25 and cites Saxe as teaching the additional limitations of claims 27 and 28. Claims 27 and 28 are patentable over the combination of Dinteman, Bhawmik, Churchill and Saxe because, as discussed above relative to claim 25, Dinteman, Churchill and Bhawmik fail to teach limitations of claim 25. The Examiner cites Saxe only as teaching the additional limitations of claims 27 and 28. Claims 27 and 28 are therefore patentable over the cited references.

24. Claims 31, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Bhawmik, Osawa, Chetlur, Churchill, and Speyer. The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

Relative to claim 31, the Examiner cites Churchill as motivating one of skill in the art to place Dinteman's programmable delay circuit within the IC being tested. As mentioned above, in order to produce jitter in a test signal (such as Churchill's signal 316) it would be necessary to supply control data to programmable delay circuit 302 that changes at the rate at which state changes in the test signal occur because it is necessary to independently control the timing of each edge of the test signal. One of skill in the art would not be motivated to use Churchill's embedded programmable delay circuit 302 to produce a jittery test signal because the scan bus could not supply data to frequency modulate input signal 314 at a sufficient rate during a test when the IC is processing test signal 316.

The Examiner cites Osawa (FIG. 1) as showing a selector circuit 233 that can selectively supply either of its two input signals as an output signal. Osawa's selector 233 is included in a scan register to select between a data signal output D of a semiconductor device and a serial signal SI from another source. Osawa's circuit has nothing to do with jitter testing and does not select between the input to a

programmable delay circuit and the jittery output of the programmable delay circuit as recited in the applicant's claim 5. Thus Osawa provides no motivation for one of skill in the art to use Osawa's selector as the recited "first means" in connection with Dinteman's jitter generator circuit.

The Examiner cites Chetlur (FIG. 1) as teaching a selector 12 that receives a test signal from a multiplexer 14 and a second signal VG to produce an input signal VIN to a "circuit path", but the selector 12 does not feed back the test signal output of a programmable delay circuit to the delay circuit's input to cause the test signal to oscillate and therefore does not suggest the "multiplexer" recited in claim 31.

The Examiner cites Speyer as teaching an oscillator formed by feeding the output of a delay circuit back to its input, and suggests that one of skill in the art would be motivated to modify Dinteman's circuit in this manner because doing so would provide an oscillating test signal. However since the output of Dinteman's programmable delay circuit is a timing signal TD' and not a test signal, one of skill in the art would not be motivated to modify Dinteman's test circuit in such manner. It would also decouple the timing of the TD' signal from the timing of other circuits within the IC tester which are synchronized to the TD signal, thereby causing the tester channel to lose synchronicity with the other tester channels. One of skill in the art would not want that. Claims 31, 34 and 35 are therefore patentable over the cited references.

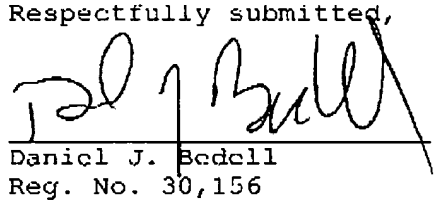
25. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman, Bhawmik, Osawa, Chetlur, Churchill, Speyer and Saxe. The Examiner is respectfully requested to withdraw the rejection in view of the following comments.

The Examiner cites Dinteman, Bhawmik, Osawa, Chetlur, Churchill, and Speyer as teaching the underlying subject matter of claim 31 and cites Saxe as teaching the additional limitations of claims 32 and 33. Claims 27 and 28 are patentable over the combination of Dinteman,

Bhawmik, Osawa, Chetlur, Churchill, Speyer and Saxe because, as discussed above relative to claim 31, Dinteman, Bhawmik, Osawa, Chetlur, Churchill, and Speyer fail to teach limitations of claim 31. The Examiner cites Saxe only as teaching the additional limitations of claims 32 and 33. Claims 32 and 33 are therefore patentable over the cited references.

In view of the foregoing amendments and remarks, it is believed the application is in condition for allowance. Notice of allowance is therefore respectfully requested.

Respectfully submitted,



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